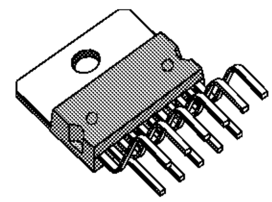
SGS-THOMSON MICROELECTRONICS

L296
L296P

HIGH CURRENT SWITCHING REGULATORS

- 4 A OUTPUT CURRENT
- 5.1 V TO 40 V OUTPUT VOLTAGE RANGE
- 0 TO 100 % DUTY CYCLE RANGE
- PRECISE (±2 %) ON-CHIP REFERENCE
- SWITCHING FREQUENCY UP TO 200 KHz
- VERY HIGH EFFICIENCY (UP TO 90 %)
- VERY FEW EXTERNAL COMPONENTS
- SOFT START
- RESET OUTPUT
- EXTERNAL PROGRAMMABLE LIMITING CURRENT (L296P)
- CONTROL CIRCUIT FOR CROWBAR SCR
- INPUT FOR REMOTE INHIBIT AND SYNCHRONUS PWM
- THERMAL SHUTDOWN



Multiwatt®
(15 lead)

ORDERING NUMBERS :

L296 (Vertical)	L296HT (Horizontal)
L296P (Vertical)	L296PHT (Horizontal)

DESCRIPTION

The L296 and L296P are stepdown power switching regulators delivering 4 A at a voltage variable from 5.1 V to 40 V.

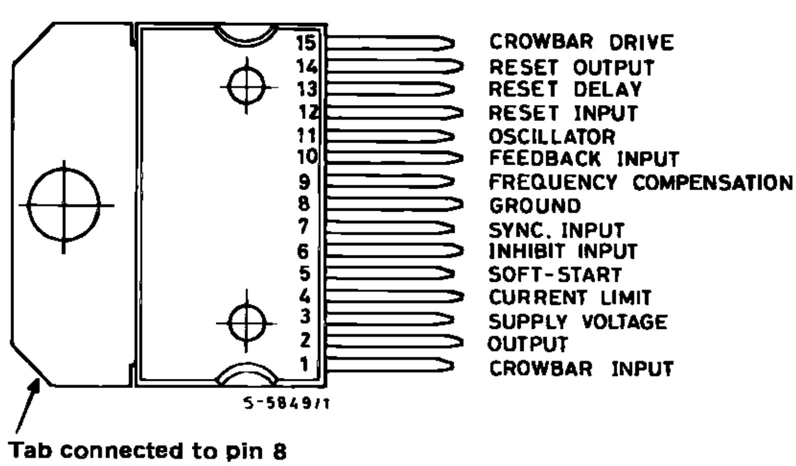
Features of the devices include soft start, remote inhibit, thermal protection, a reset output for microprocessors and a PWM comparator input for synchronization in multichip configurations.

The L296P incudes external programmable limiting current.

The L296 and L296P are mounted in a 15-lead Multiwatt® plastic power package and requires very few external components.

Efficient operation at switching frequencies up to 200 KHz allows a reduction in the size and cost of external filter components. A voltage sense input and SCR drive output are provided for optional crowbar overvoltage protection with an external SCR.

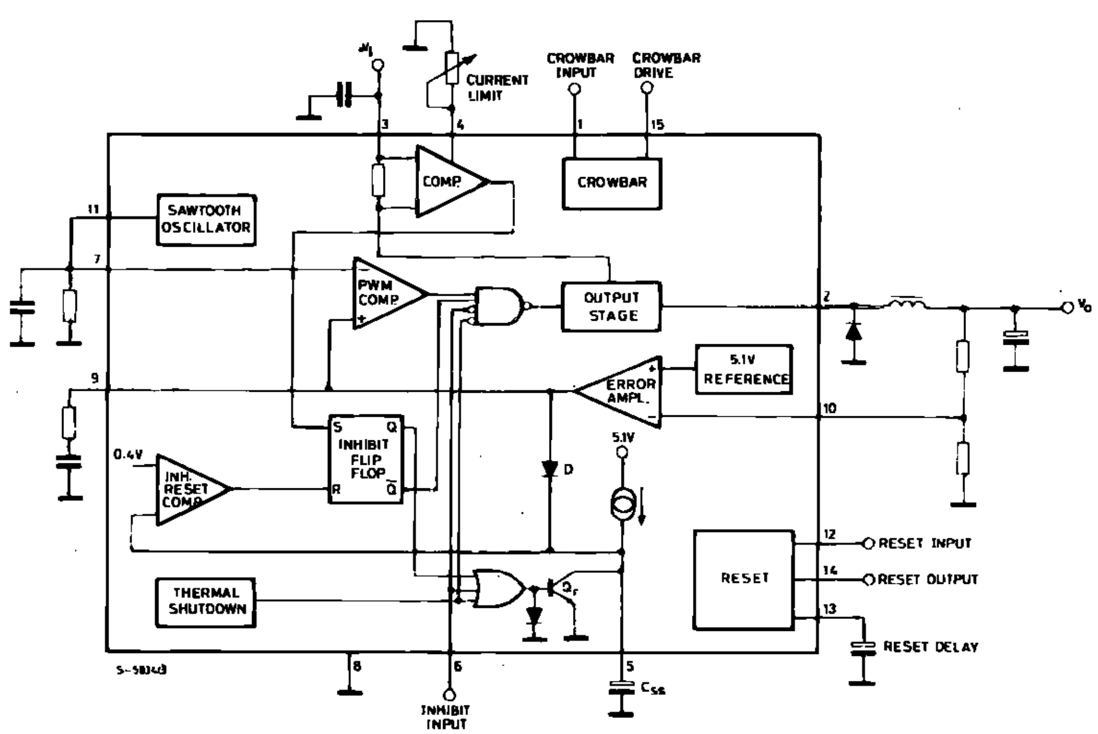
PIN CONNECTION (top view)



PIN FUNCTIONS

N°	Name	Function
1	CROWBAR INPUT	Voltage Sense Input for Crowbar Overvoltage Protection. Normally connected to the feedback input thus triggering the SCR when V_{out} exceeds nominal by 20 %. May also monitor the input and a voltage divider can be added to increase the threshold. Connected to ground when SCR not used.
2	OUTPUT	Regulator Output
3	SUPPLY VOLTAGE	Unrergulated Voltage Input. An internal Regulator Powers the L296s Internal Logic.
4	CURRENT LIMIT	A resistor connected between this terminal and ground sets the current limiter threshold. If this terminal is left unconnected the threshold is internally set (see electrical characteristics).
5	SOFT START	Soft Start Time Constant. A capacitor is connected between this terminal and ground to define the soft start time constant. This capacitor also determines the average short circuit output current.
6	INHIBIT INPUT	TTL – Level Remote Inhibit. A logic high level on this input disables the device.
7	SYNC INPUT	Multiple L296s are synchronized by connecting the pin 7 inputs together and omitting the oscillator RC network on all but one device.
8	GROUND	Common Ground Terminal
9	FREQUENCY COMPENSATION	A series RC network connected between this terminal and ground determines the regulation loop gain characteristics.
10	FEEDBACK INPUT	The Feedback Terminal on the Regulation Loop. The output is connected directly to this terminal for 5.1V operation ; it is connected via a divider for higher voltages.
11	OSCILLATOR	A parallel RC networki connected to this terminal determines the switching frequency. This pin must be connected to pin 7 input when the internal oscillator is used.
12	RESET INPUT	Input of the Reset Circuit. The threshold is roughly 5 V. It may be connected to the feedback point or via a divider to the input.
13	RESET DELAY	A capacitor connected between this terminal and ground determines the reset signal delay time.
14	RESET OUTPUT	Open collector reset signal output. This output is high when the supply is safe.
15	CROWBAR OUTPUT	SCR gate drive output of the crowbar circuit.

BLOCK DIAGRAM



CIRCUIT OPERATION

(refer to the block diagram)

The L296 and L296P are monolithic stepdown switching regulators providing output voltages from 5.1V to 40V and delivering 4A.

The regulation loop consists of a sawtooth oscillator, error amplifier, comparator and the output stage. An error signal is produced by comparing the output voltage with a precise 5.1V on-chip reference (zener zap trimmed to ± 2 %). This error signal is then compared with the sawtooth signal to generate the fixed frequency pulse width modulated pulses which drive the output stage. The gain and frequency stability of the loop can be adjusted by an external RC network connected to pin 9. Closing the loop directly gives an output voltage of 5.1V. Higher voltages are obtained by inserting a voltage divider.

Output overcurrents at switch on are prevented by the soft start function. The error amplifier output is initially clamped by the external capacitor Css and allowed to rise, linearly, as this capacitor is charged by a constant current source.

Output overload protection is provided in the form of a current limiter. The load current is sensed by an internal metal resistor connected to a comparator. When the load current exceeds a preset threshold this comparator sets a flip flop which disables the output stage and discharges the soft start capacitor. A second comparator resets the flip flop when the voltage across the soft start capacitor has fallen to 0.4V. The output stage is thus re-enabled and the output voltage rises under control of the soft start network. If the overload condition is still present the limiter will trigger again when the threshold current is reached. The average short circuit current is limited to a safe value by the dead time introduced by the soft start network.

The reset circuit generates an output signal when the supply voltage exceeds a threshold programmed by an external divider. The reset signal is generated with a delay time programmed by an external capacitor. When the supply falls below the threshold the reset output goes low immediately. The reset output is an open collector.

The scrowbar circuit senses the output voltage and the crowbar output can provide a current of 100mA to switch on an external SCR. This SCR is triggered when the output voltage exceeds the nominal by 20%. There is no internal connection between the output and crowbar sense input therefore the crowbar can monitor either the input or the output.

A TTL - level inhibit input is provided for applications such as remote on/off control. This input is activated by high logic level and disables circuit operation. After an inhibit the L296 restarts under control of the soft start network.

The thermal overload circuit disables circuit operation when the junction temperature reaches about 150 °C and has hysteresis to prevent unstable conditions.

Figure 1 : Reset Output Waveforms

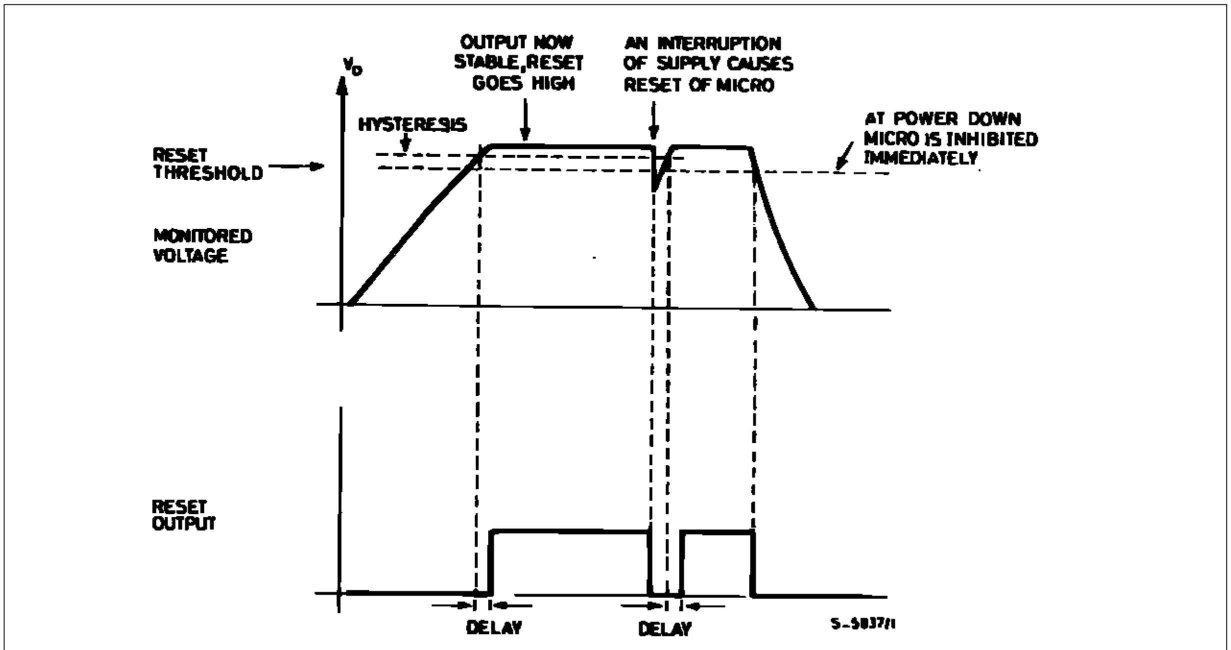


Figure 2 : Soft Start Waveforms

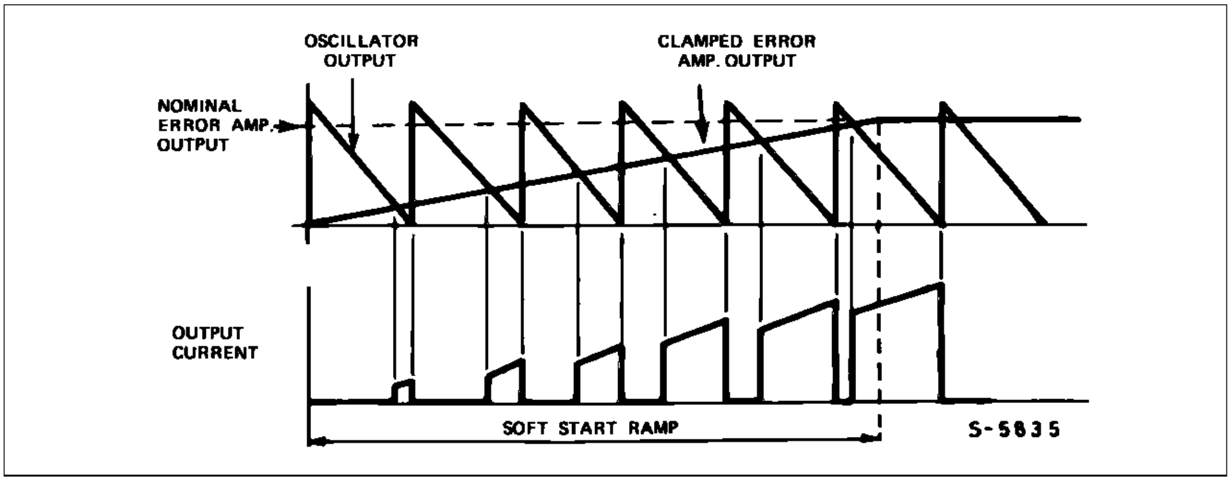
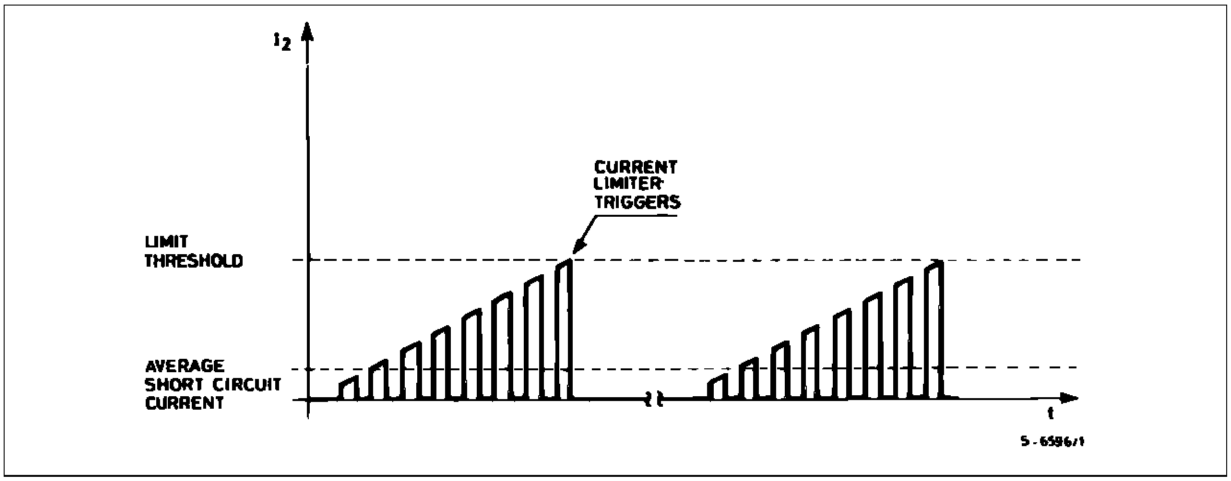


Figure 3 : Current Limiter Waveforms



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	Input Voltage (pin 3)	50	V
$V_i - V_2$	Input to Output Voltage Difference	50	V
V_2	Output DC Voltage Output Peak Voltage at t = 0.1 µsec f = 200KHz	– 1 – 7	V V
V_1, V_{12}	Voltage at Pins 1, 12	10	V
V_{15}	Voltage at Pin 15	15	V
V_4, V_5, V_7, V_9, V_{13}	Voltage at Pins 4, 5, 7, 9 and 13	5.5	V
V_{10}, V_6	Voltage at Pins 10 and 6	7	V
V_{14}	Voltage at Pin 14 ($I_{14} \leq 1$ mA)	V_i	
I_9	Pin 9 Sink Current	1	mA
I_{11}	Pin 11 Source Current	20	mA
I_{14}	Pin 14 Sink Current ($V_{14} < 5$ V)	50	mA
P_{tot}	Power Dissipation at $T_{case} \leq 90$ °C	20	W
T_j, T_{stg}	Junction and Storage Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	35	°C/W

ELECTRICAL CHARACTERISTICS

(refer to the test circuits $T_j = 25^oC$, $V_i = 35V$, unless otherwise specified)

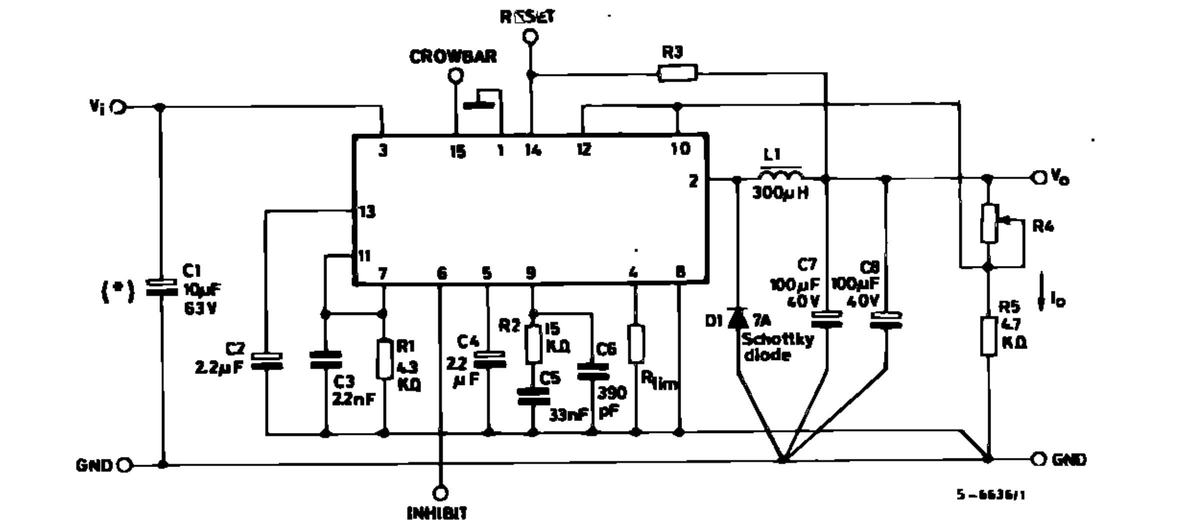
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
DYNAMIC CHARACTERISTICS (pin 6 to GND unless otherwise specified)							
V_o	Output Voltage Range	V_i = 46V, I_o = 1A	V_{ref}		40	V	4
V_i	Input Voltage Range	$V_o = V_{ref}$ to 36V, $I_o \leq$ 3A	9		46	V	4
V_i	Input Voltage Range	Note (1), $V_o = V_{REF}$ to 36V I_o = 4A			46	V	4
ΔV_o	Line Regulation	V_i =10V to 40V, $V_o = V_{ref}$, I_o = 2A		15	50	mV	4
ΔV_o	Load Regulation	$V_o = V_{ref}$ I_o = 2A to 4A I_o = 0.5A to 4A		 10 15	 30 45	mV	4
V_{ref}	Internal Reference Voltage (pin 10)	V_i = 9V to 46V, I_o = 2A	5	5.1	5.2	V	4
$\frac{\Delta V_{ref}}{\Delta T}$	Average Temperature Coefficient of Reference Voltage	T_j = 0°C to 125°C, I_o = 2A		0.4		mV/°C	
V_d	Dropout Voltage Between Pin 2 and Pin 3	I_o = 4A I_o = 2A		2 1.3	3.2 2.1	V V	4 4
I_{2L}	Current Limiting Threshold (pin 2)	L296 - Pin 4 Open, V_i = 9V to 40V, $V_o = V_{ref}$ to 36V	4.5		7.5	A	4
		L296P - V_i = 9V to 40V, $V_o = V_{ref}$ Pin 4 Open R_{lim} = 22kΩ	 5 2.5		 7 4.5	A	4
I_{SH}	Input Average Current	V_i = 46V, Output Short-circuited		60	100	mA	4
η	Efficiency	I_o = 3 A $V_o = V_{ref}$ V_o = 12V		 75 85		%	4
SVR	Supply Voltage Ripple Rejection	ΔV_i = 2 V_{rms}, f_{ripple} = 100Hz $V_o = V_{ref}$, I_o = 2A	50	56		dB	4
f	Switching Frequency		85	100	115	kHz	4
$\frac{\Delta f}{\Delta V_i}$	Voltage Stability of Switching Frequency	V_i = 9V to 46V		0.5		%	4
$\frac{\Delta f}{\Delta T_j}$	Temperature Stability of Switching Frequency	T_j = 0°C to 125°C		1		%	4
f_{max}	Maximum Operating Switching Frequency	$V_o = V_{ref}$, I_o = 1A	200			kHz	–
T_{sd}	Thermal Shutdown Junction Temperature	Note (2)	135	145		°C	–
DC CHARACTERISTICS							
I_{3Q}	Quiescent Drain Current	V_i = 46V, V_7 = 0V, S1 : B, S2 : B V_6 = 0V V_6 = 3V			 66 30	 85 40	mA
– I_{2L}	Output Leakage Current	V_i = 46V, V_6 = 3V, S1 : B, S2 : A, V_7 = 0V				2	mA

Note (1) : Using min. 7 A schottky diode.
(2) : Guaranteed by design, not 100 % tested in production.

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit	Fig.
SOFT START							
$I_{5\ so}$	Source Current	V_6 = 0V, V_5 = 3V	80	130	150	μA	6b
$I_{5\ si}$	Sink Current	V_6 = 3V, V_5 = 3V	50	70	120	μA	6b
INHIBIT							
 V_{6L} V_{6H}	Input Voltage Low Level High Level	V_i = 9V to 46V, V_7 = 0V, S1 : B, S2 : B	 – 0.3 2		 0.8 5.5	V	6a
  – I_{6L} – I_{6H}	Input Current with Input Voltage Low Level High Level	V_i = 9V to 46V, V_7 = 0V, S1 : B, S2 : B V_6 = 0.8V V_6 = 2V			 10 3	μA	6a
ERROR AMPLIFIER							
V_{9H}	High Level Output Voltage	V_{10} = 4.7V, I_9 = 100μA, S1 : A, S2 : A	3.5			V	6c
V_{9L}	Low Level Output Voltage	V_{10} = 5.3V, I_9 = 100μA, S1 : A, S2 : E			0.5	V	6c
$I_{9\ si}$	Sink Output Current	V_{10} = 5.3V, S1 : A, S2 : B	100	150		μA	6c
– $I_{9\ so}$	Source Output Current	V_{10} = 4.7V, S1 : A, S2 : D	100	150		μA	6c
I_{10}	Input Bias Current	V_{10} = 5.2V, S1 : B V_{10} = 6.4V, S1 : B, L296P		2 2	10 10	μA μA	6c 6c
G_v	DC Open Loop Gain	V_9 = 1V to 3V, S1 : A, S2 : C	46	55		dB	6c
OSCILLATOR AND PWM COMPARATOR							
– I_7	Input Bias Current of PWM Comparator	V_7 = 0.5V to 3.5V			5	μA	6a
– I_{11}	Oscillator Source Current	V_{11} = 2V, S1 : A, S2 : B	5			mA	
RESET							
$V_{12\ R}$	Rising Threshold Voltage	V_i = 9V to 46V, S1 : B, S2 : B	V_{ref} -150mV	V_{ref} -100mV	V_{ref} -50mV	V	6d
$V_{12\ F}$	Falling Threshold Voltage		4.75	V_{ref} -150mV	V_{ref} -100mV	V	6d
$V_{13\ D}$	Delay Thershold Voltage	V_{12} = 5.3V, S1 : A, S2 : B	4.3	4.5	4.7	V	6d
$V_{13\ H}$	Delay Threshold Voltage Hysteresis			100		mV	6d
$V_{14\ S}$	Output Saturation Voltage	I_{14} = 16mA, V_{12} = 4.7V, S1, S2 : B			0.4	V	6d
I_{12}	Input Bias Current	V_{12} = 0V to V_{ref}, S1 : B, S2 : B		1	3	μA	6d
 – $I_{13\ so}$ $I_{13\ si}$	 Delay Source Current Delay Sink Current	V_{13} = 3V, S1 : A, S2 : B V_{12} = 5.3V V_{12} = 4.7V	 70 10	 110	 140	 μA mA	6d
I_{14}	Output Leakage Current	V_i = 46V, V_{12} = 5.3V, S1 : B, S2 : A			100	μA	6d
CROWBAR							
V_1	Input Threshold Voltage	S1 : B	5.5	6	6.4	V	6b
V_{15}	Output Saturation Voltage	V_i = 9V to 46V, V_i = 5.4V, I_{15} = 5mA, S1 : A		0.2	0.4	V	6b
I_1	Input Bias Current	V_1 = 6V, S1 : B			10	μA	6b
– I_{15}	Output Source Current	V_i = 9V to 46V, V_1 = 6.5V, V_{15} = 2V, S1 : B	70	100		mA	6b

Figure 4 : Dynamic Test Circuit



C7, C8 : EKR (ROE)
L1 : L = 300 µH at 8 A Core type : MAGNETICS 58930 - A2 MPP
N° turns : 43 Wire Gauge : 1 mm (18 AWG) COGEMA 946044
(*) Minimum suggested value (10 µF) to avoid oscillations. Ripple consideration leads to typical value of 1000 µF or higher.

Figure 5 : PC. Board and Component Layout of the Circuit of Figure 4 (1:1 scale)

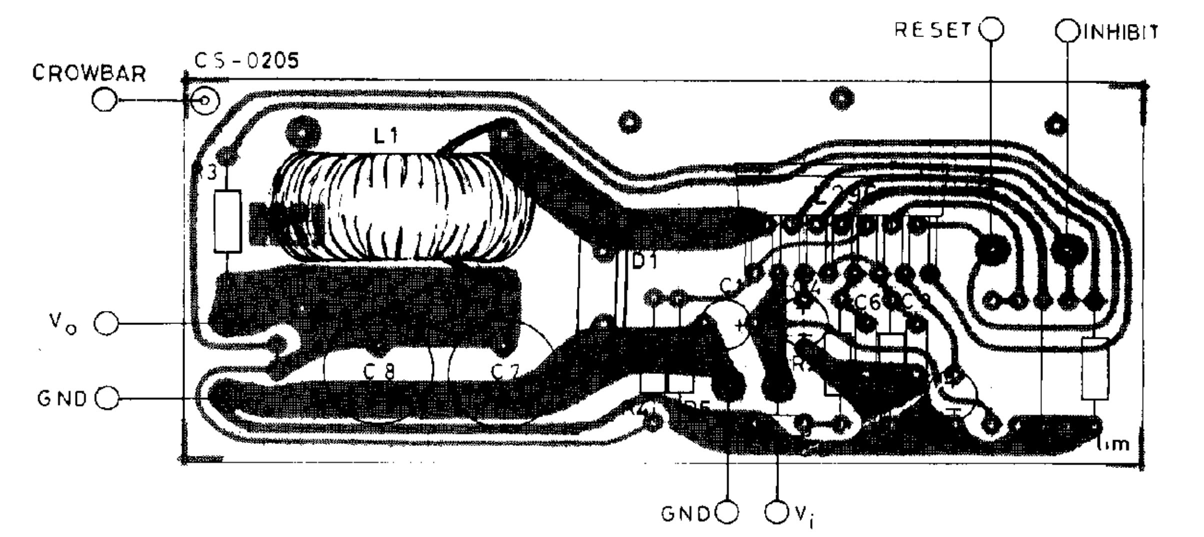


Figure 6 : DC Test Circuits.

Figure 6a.

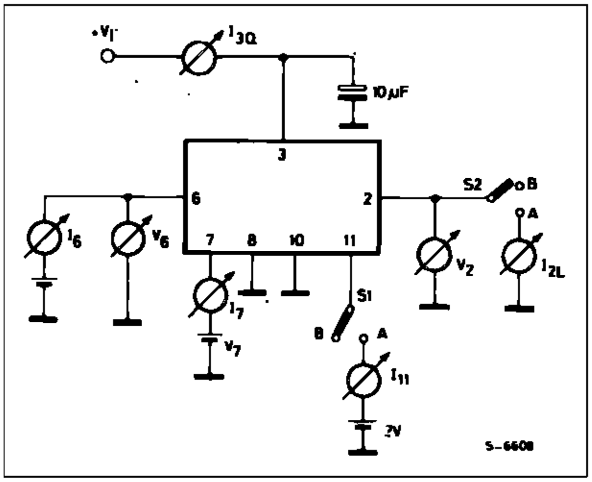


Figure 6b.

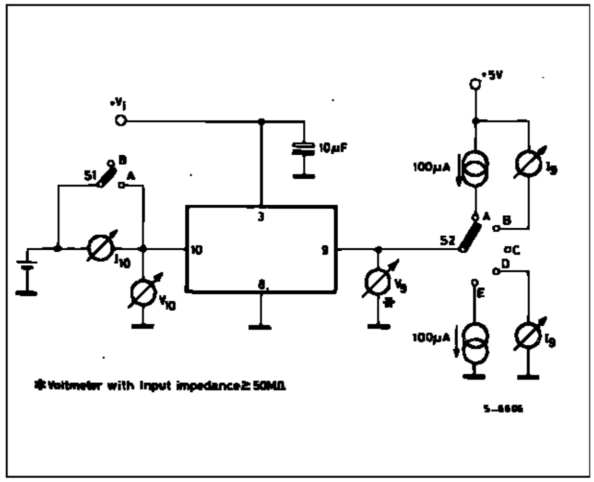
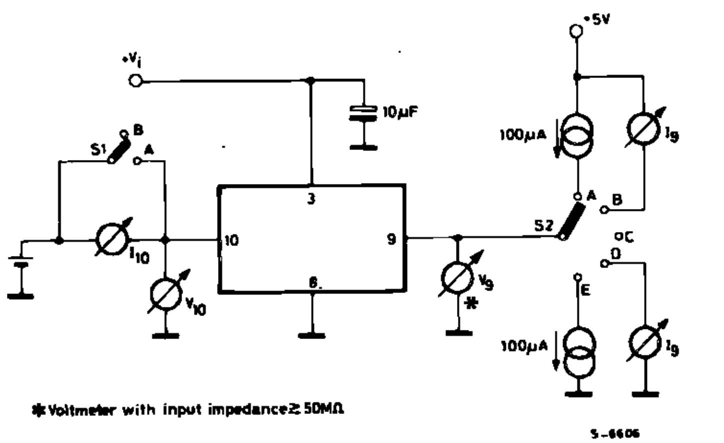


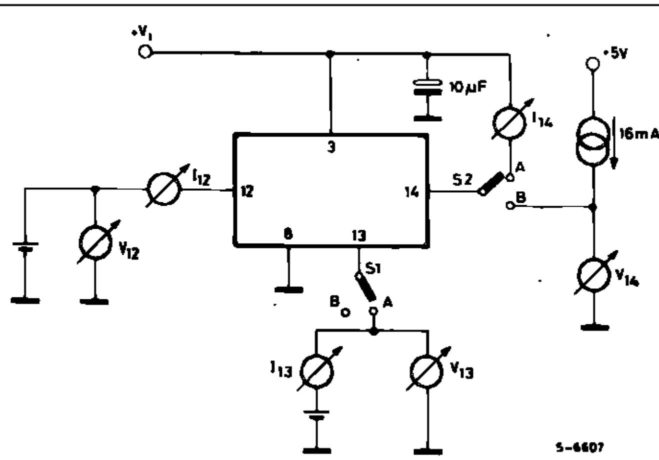
Figure 6c.



1 - Set V_{10} FOR V_9 = 1 V
2 - Change V_{10} to obtain V_9 = 3 V

3 - $G_V = \frac{DV_9}{\Delta V_{10}} = \frac{2V}{\Delta V_{10}}$

Figure 6d.



SGS-THOMSON MICROELECTRONICS

Figure 7 : Quienscent Drain Current vs. Supply Voltage (0 % Duty Cycle - see fig. 6a).

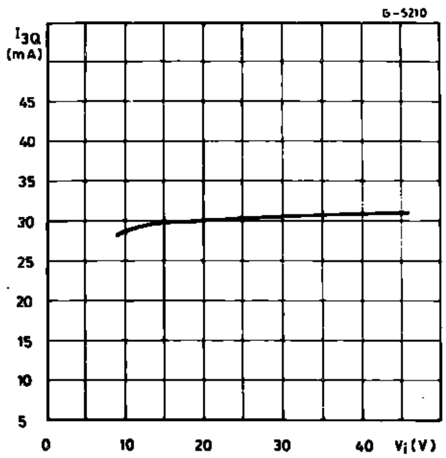


Figure 8 : Quienscent Drain Current vs. Supply Voltage (100 % Duty Cycle see fig. 6a).

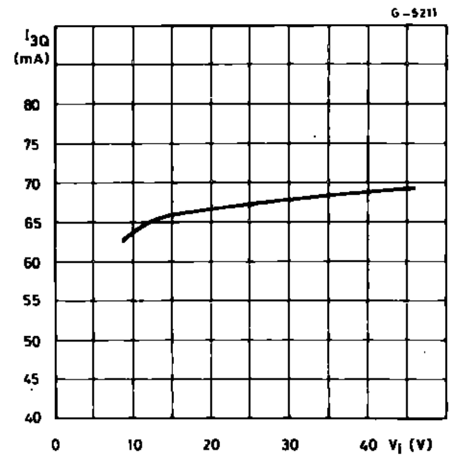


Figure 9 : Quiescent Drain Current vs. Junction Temperature (0 % Duty Cycle - see fig. 6a).

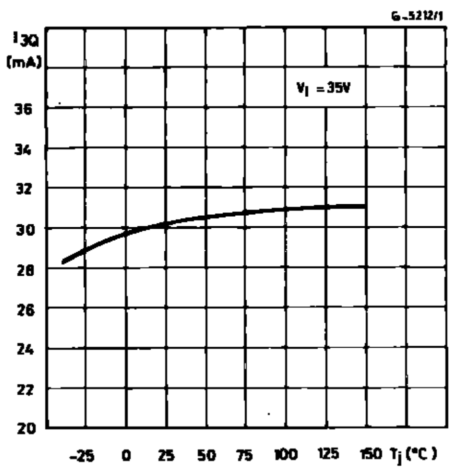


Figure 10 : Quiescent Drain Current vs. Junction Temperature (100 % Duty Cycle - see fig. 6a).

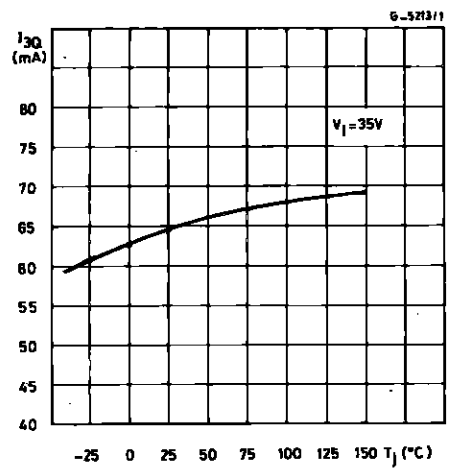


Figure 11 : Reference Voltage (pin 10) vs. V_I (see fig. 4).

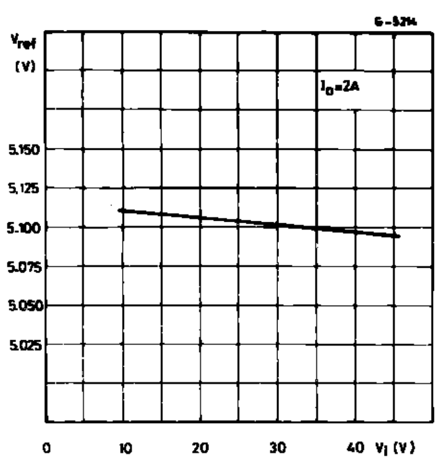


Figure 12 : Reference Voltage (pin 10) vs. Junction Temperature (see fig. 4).

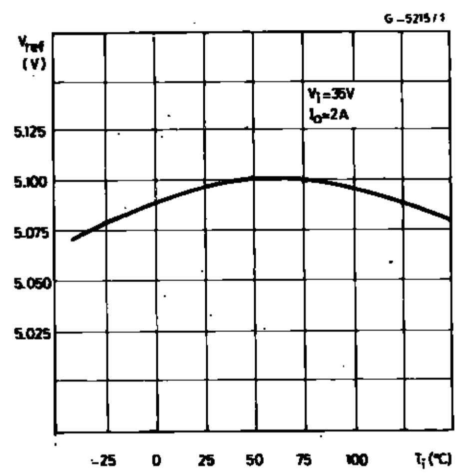


Figure 13 : Open Loop Frequency and Phase Response of Error Amplifier (see fig. 6c).

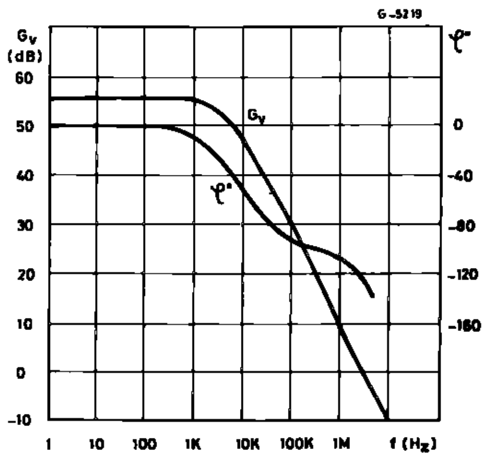


Figure 14 : Switching Frequency vs. Input Voltage (see fig. 4).

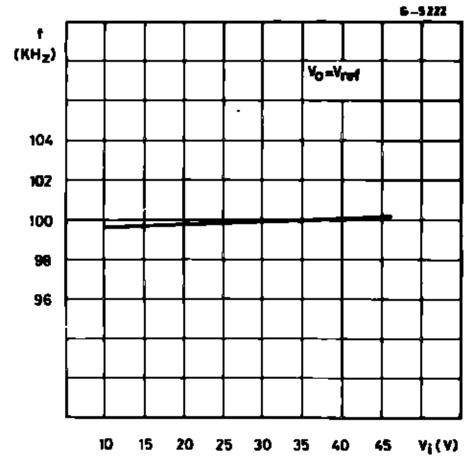


Figure 15 : Switching Frequency vs. Junction Temperature (see fig. 4).

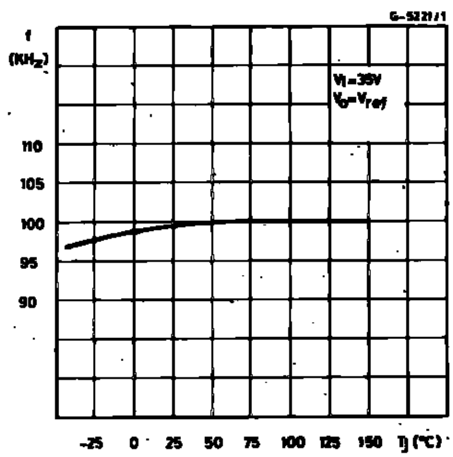


Figure 16 : Switching Frequency vs. R1 (see fig. 4).

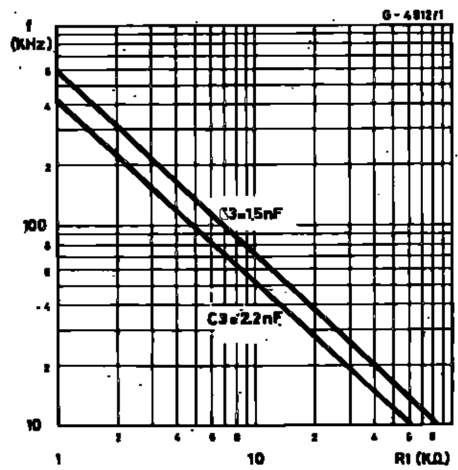


Figure 17 : Line Transient Response (see fig. 4).

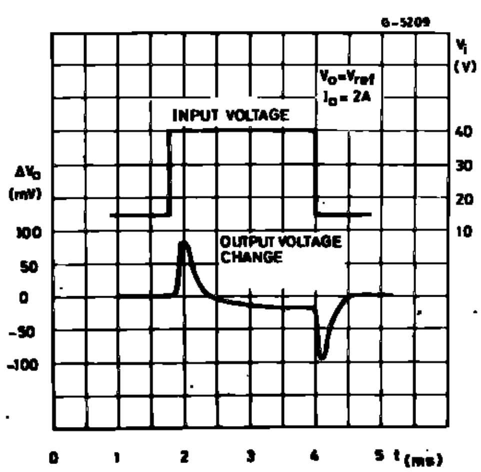


Figure 18 : Load Transient Response (see fig. 4).

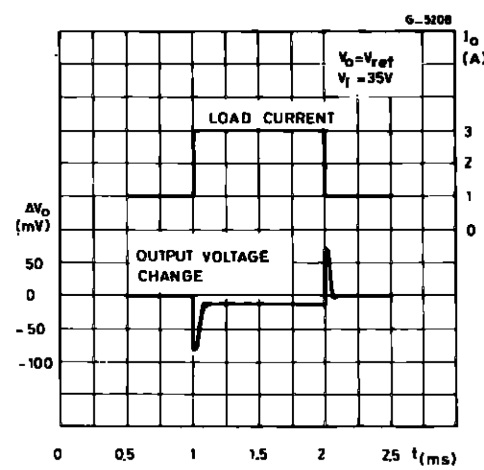


Figure 19 : Supply Voltage Ripple Rejection vs. Frequency (see fig. 4).

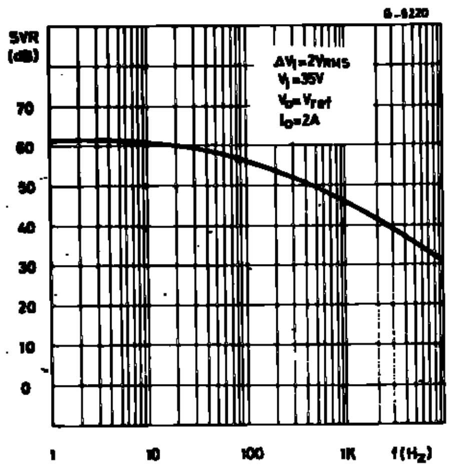


Figure 20 : Dropout Voltage Between Pin 3 and Pin 2 vs. Current at Pin 2.

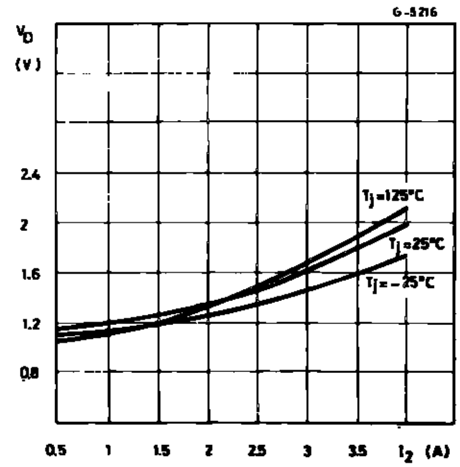


Figure 21 : Dropout Voltage Between Pin 3 and Pin 2 vs. Junction Temperature.

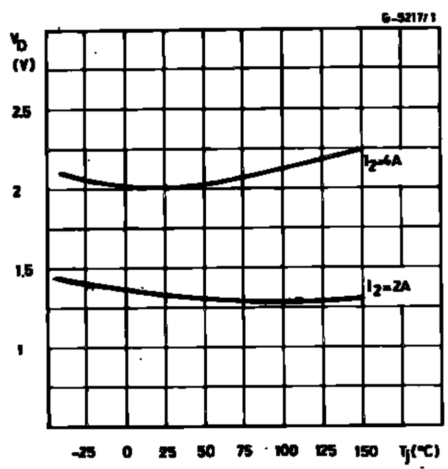


Figure 22 : Power Dissipation Derating Curve.

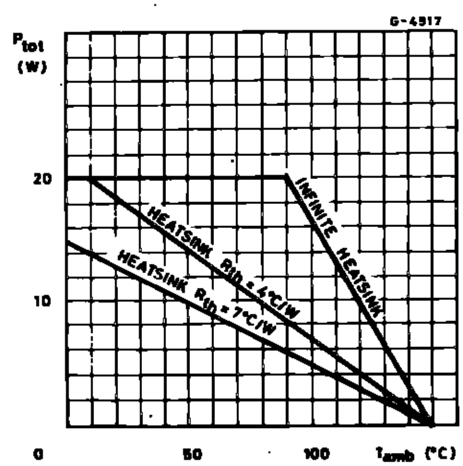


Figure 23 : Power Dissipation (device only) vs. Input Voltage.

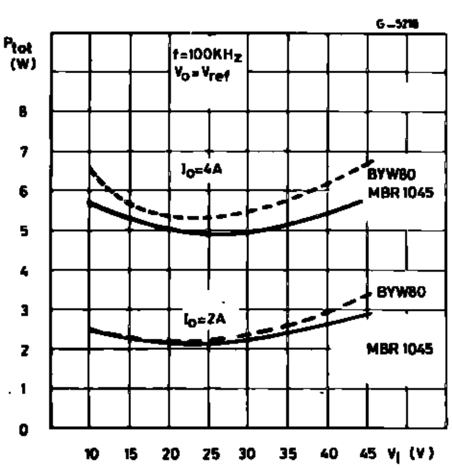


Figure 24 : Power Dissipation (device only) vs. Input voltage.

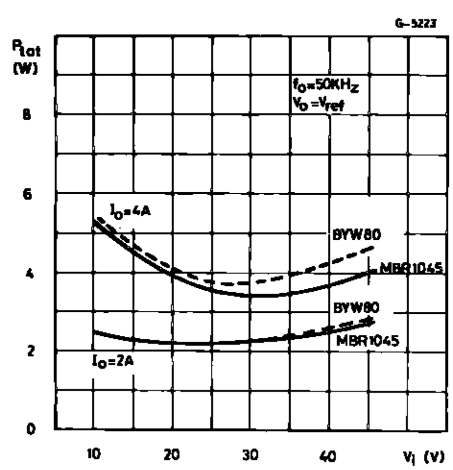


Figure 25 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

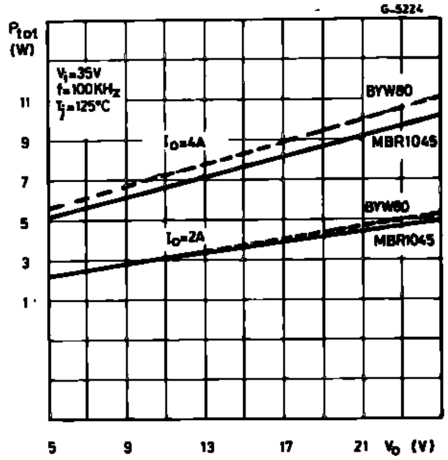


Figure 26 : Power Dissipation (device only) vs. Output Voltage (see fig. 4).

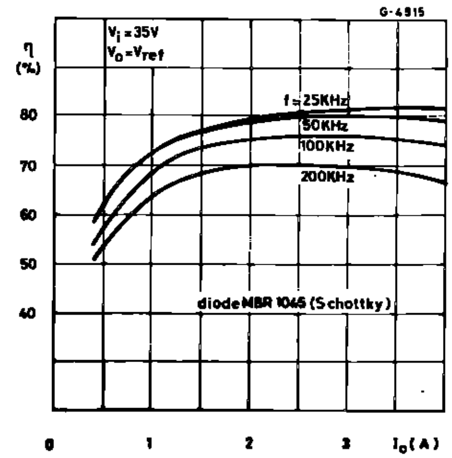


Figure 27 : Voltage and Current Waveforms at Pin 2 (see fig. 4).

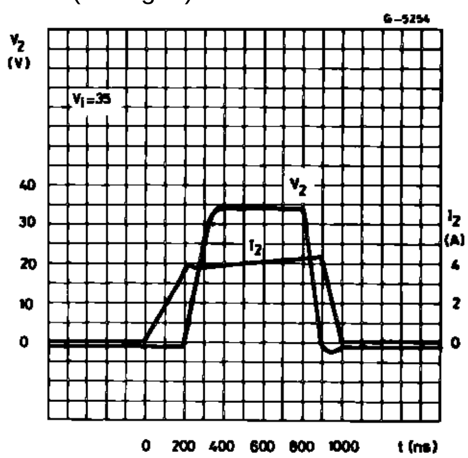


Figure 28 : Efficiency vs. Output Current.

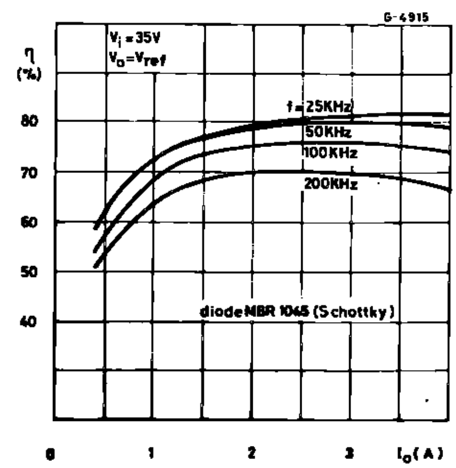


Figure 29 : Efficiency vs. Output Voltage.

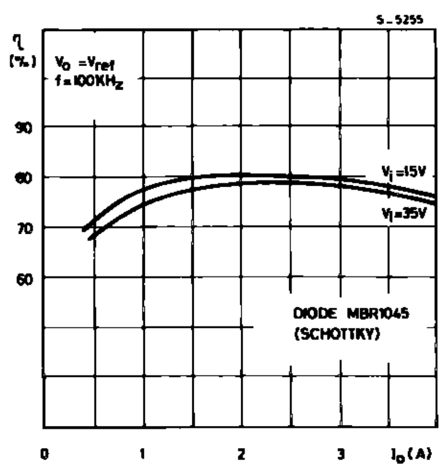


Figure 30 : Efficiency vs. Output Voltage.

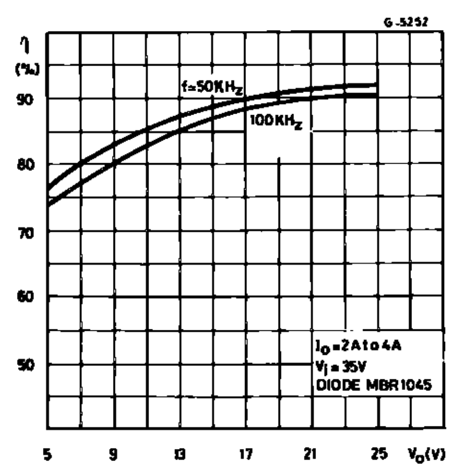


Figure 31 : Current Limiting Threshold vs. $R_{pin\ 4}$ (L296P only).

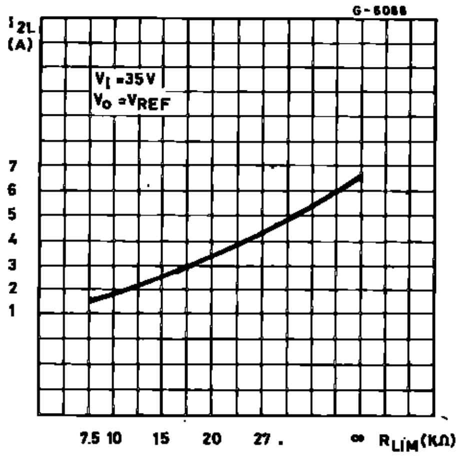


Figure 32 : Current Limiting Threshold vs. Junction Temperature.

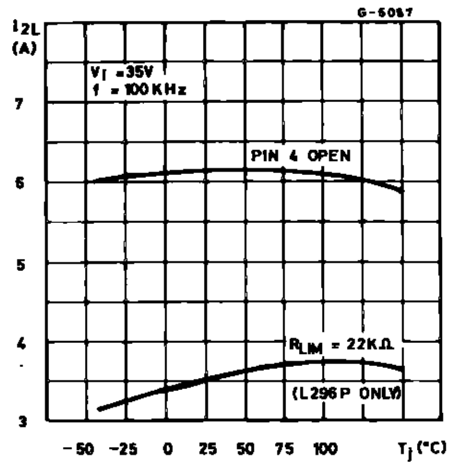
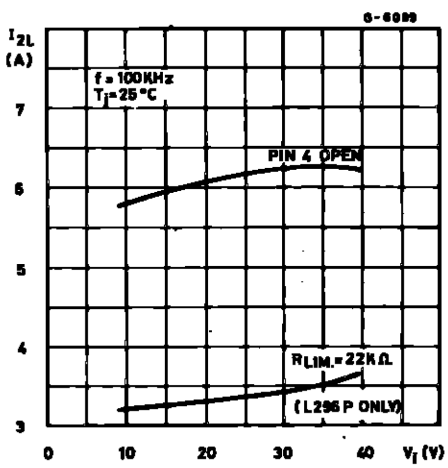
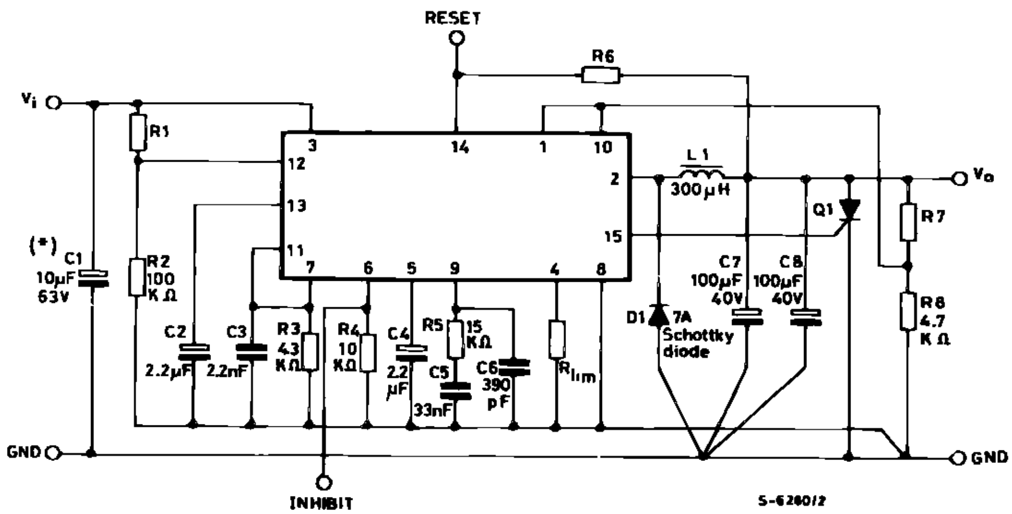


Figure 33 : Current Limiting Threshold vs. Supply Voltage.



APPLICATION INFORMATION

Figure 34 : Typical Application Circuit.



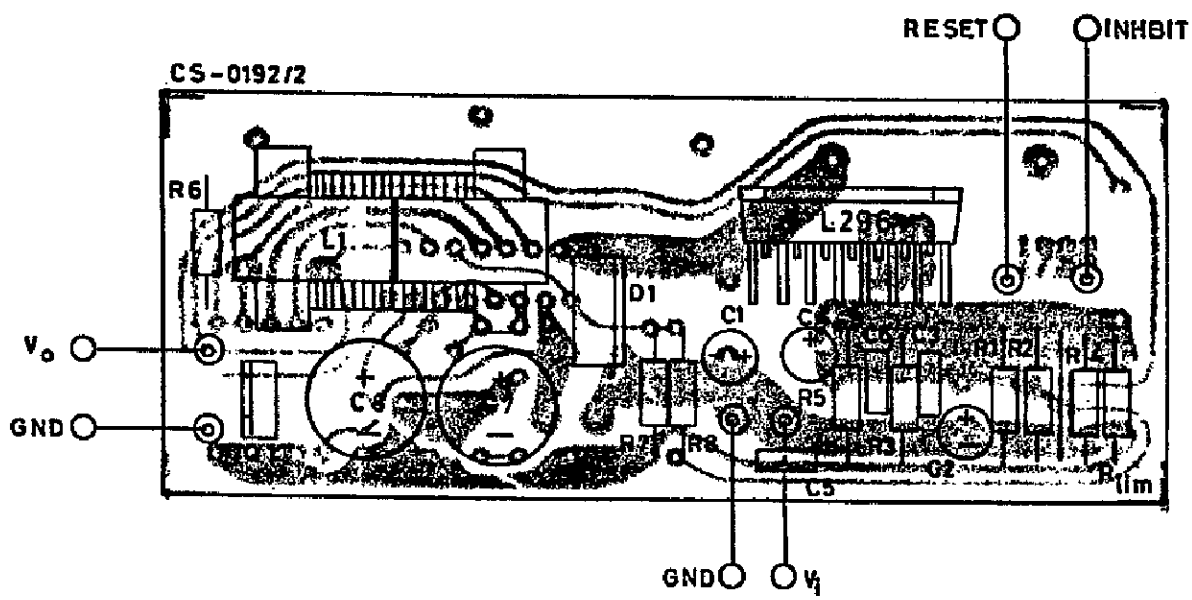
(*) Minimum value (10 µF) to avoid oscillations ; ripple consideration leads to typical value of 1000 µF or higher L1 : 58930 - MPP COGEMA 946044 ; GUP 20 COGEMA 946045

SUGGESTED INDUCTOR (L1)

Core Type	No Turns	Wire Gauge	Air Gap
Magnetics 58930 – A2MPP	43	1.0 mm	–
Thomson GUP 20 x 16 x 7	65	0.8 mm	1 mm
Siemens EC 35/17/10 (B6633& – G0500 – X127)	40	2 x 0.8 mm	–
VOGT 250 µH Toroidal Coil, Part Number 5730501800			

Resistor Values for Standard Output Voltages		
V_0	R8	R7
12 V	4.7 KΩ	6.2 KΩ
15 V	4.7 KΩ	9.1 KΩ
18 V	4.7 KΩ	12 KΩ
24 V	4.7 KΩ	18 KΩ

Figure 35 : P.C. Board and Component Layout of the Circuit of fig. 34 (1:1 scale)



SELECTION OF COMPONENT VALUES (see fig. 34)

Component	Recommended Value	Purpose	Allowed Rage		Notes
			Min.	Max.	
R1 R2	– 100 kΩ	Set Input Voltage Threshold for Reset.	–	220kΩ	R1/R2 $\frac{V_{i\,min}}{5} - 1$ If output voltage is sensed R1 and R2 may be limited and pin 12 connected to pin 10.
R3	4.3 kΩ	Sets Switching Frequency	1 kΩ	100kΩ	
R4	10 kΩ	Pull-down Resistor		22kΩ	May be omitted and pin 6 grounded if inhibit not used.
R5	15 kΩ	Frequency Compensation	10kΩ		
R6		Collector Load For Reset Output	$\frac{V_O}{0.05A}$		Omitted if reset function not used.
R7 R8	– 4.7 kΩ	Divider to Set Output Voltage	– –	– 1kΩ	R7/R8 = $\frac{V_O - V_{REF}}{V_{REF}}$ -
R_{iim}	–	Sets Current Limit Level	7.5kΩ		If R_{iim} is omitted and pin 4 left open the current limit is internally fixed.
C1	10 µF	Stability	2.2µF		
C2	2.2 µF	Sets Reset Delay	–	–	Omitted if reset function not used.
C3	2.2 nF	Sets Switching Frequency	1 nF	3.3nF	
C4	2.2 µF	Soft Start	1 µF	–	Also determines average short circuit current.
C5	33 nF	Frequency Compensation			
C6	390 pF	High Frequency Compensation	–	–	Not required for 5 V operation.
C7, C8 L1	100 µF 300 µH	Output Filter	– 100µH	–	
Q1		Crowbar Protection			The SCR must be able to withstand the peak discharge current of the output capacitor and the short circuit current of the device.
D1		Recirculation Diode			7A Schottky or 35 ns t_{rr} Diode.

Figure 36 : A Minimal 5.1 V Fixed Regulator. Very Few Components are Required.

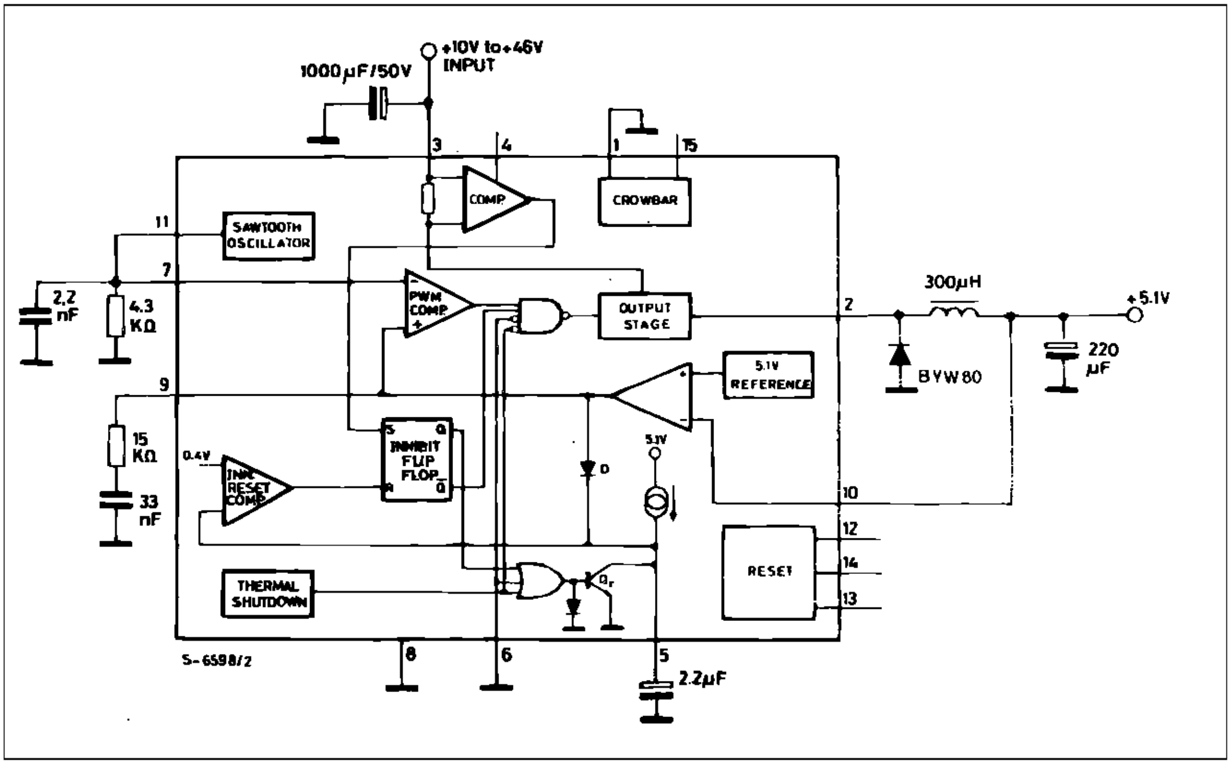


Figure 37 : 12 V/10 A Power Supply.

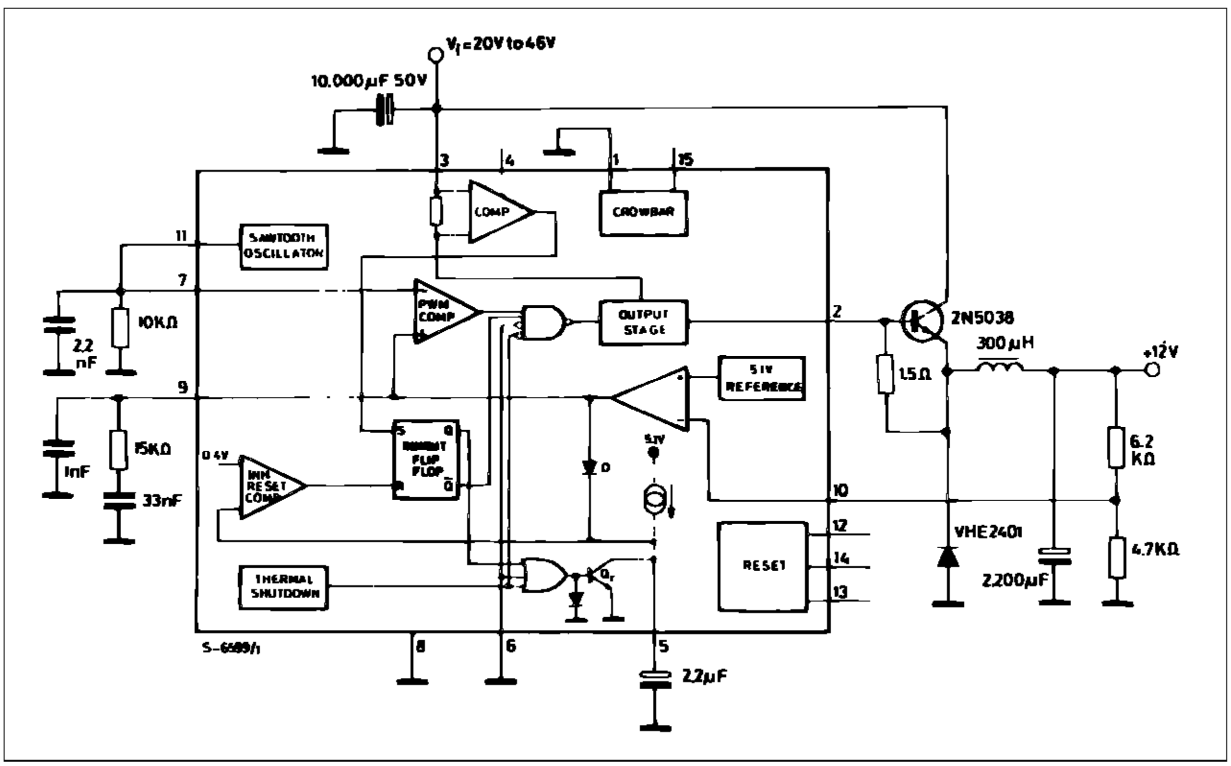
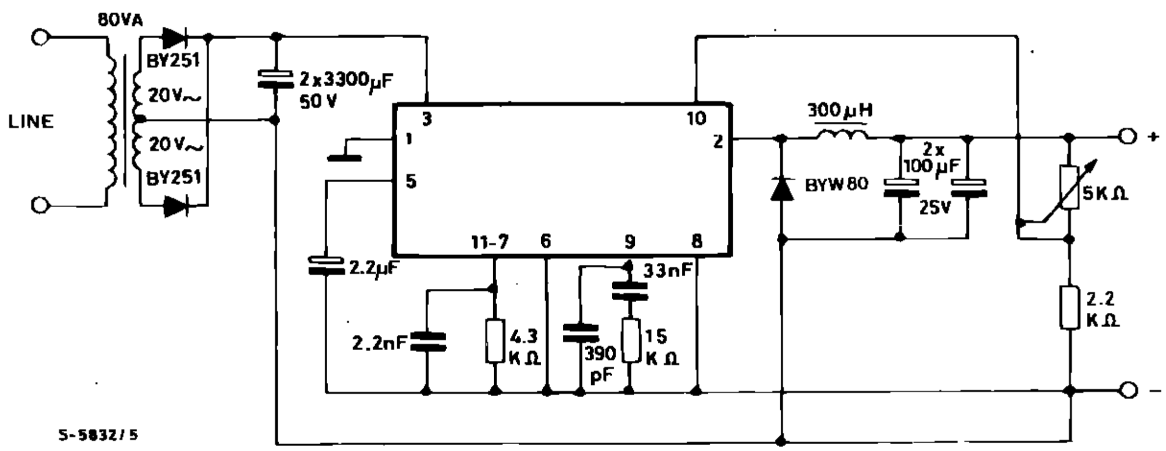
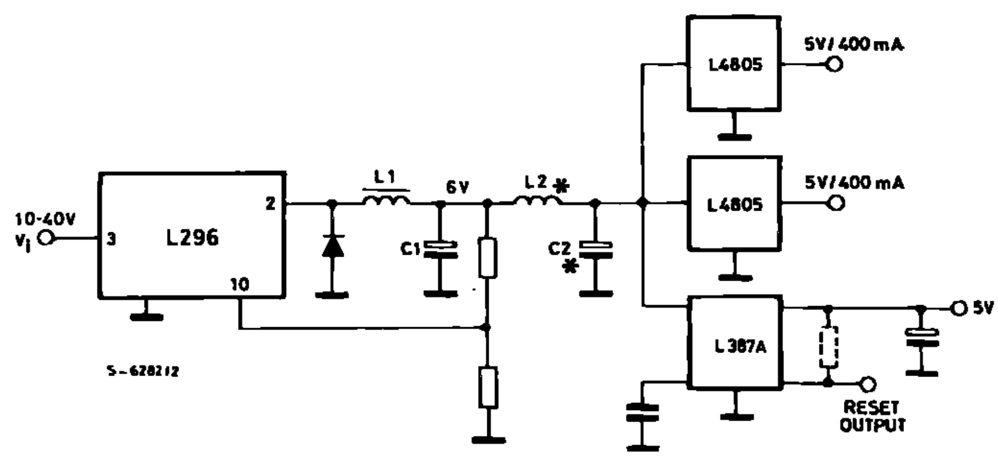


Figure 38 : Programmable Power Supply.



V o = 5.1 to 15 V
I o = 4 A max. (min. load current = 100 mA)
ripple ≤ 20 mV
load regulation (1 A to 4 A) = 10 mV (V o = 5.1 V)
line regulation (220 V ± 15 % and to I o = 3 A) = 15 mV (V o = 5.1 V)

Figure 39 : Preregulator for Distributed Supplies.



(*) L2 and C2 are necessary to reduce the switching frequency spikes.

Figure 40 : In Multiple Supplies Several L296s can be Synchronized As Shown.

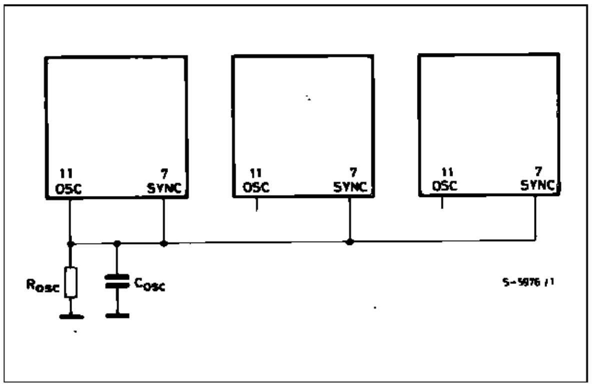


Figure 41 : Voltage Sensing for Remote Load.

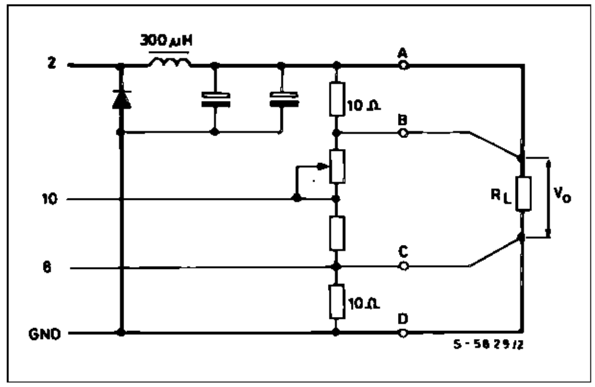


Figure 42 : A 5.1 V/15 V/24 V Multiple Supply. Note the Synchronization of the Three L296s.

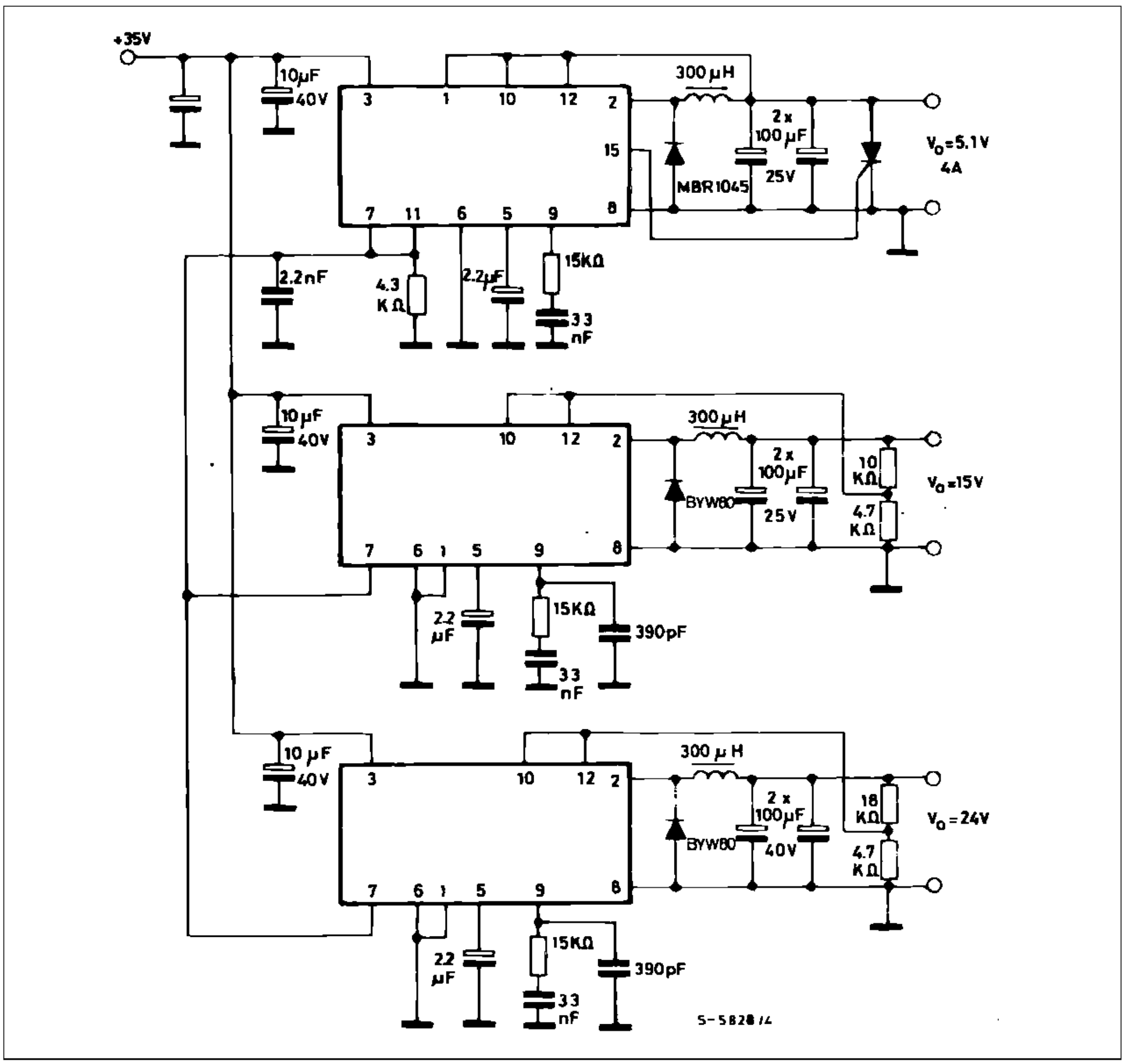
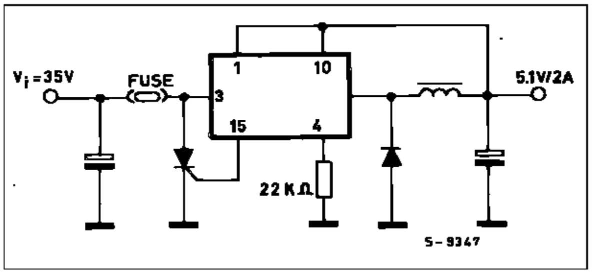


Figure 43 : 5.1V/2A Power Supply using External Limiting Current Resistor and Crowbar Protection on the Supply Voltage (L296P only)

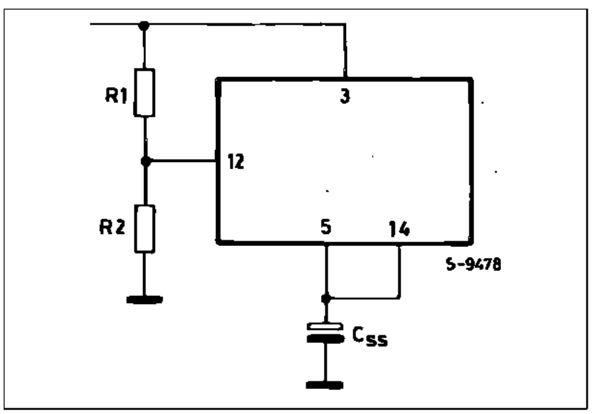


SOFT-START AND REPETITIVE POWER-ON

When the device is repetitively powered-on, the soft-start capacitor, C_{SS}, must be discharged rapidly to ensure that each start is "soft". This can be achieved economically using the reset circuit, as shown in Figure 44.

In this circuit the divider R1, R2 connected to pin 12 determines the minimum supply voltage, below which the open collector transistor at the pin 14 output discharges C_{SS}.

Figure 44

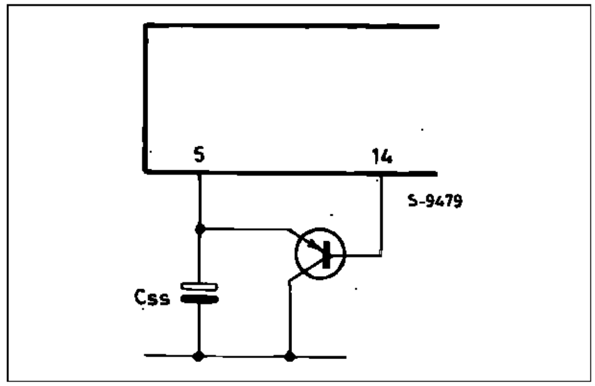


The approximate discharge times obtained with this circuit are :

CSS (µF)	tDIS (µs)
2.2	200
4.7	300
10	600

If these times are still too long, an external PNP transistor may be added, as shown in Figure 45 ; with this circuit discharge times of a few microseconds may be obtained.

Figure 45



HOW TO OBTAIN BOTH RESET AND POWER FAIL

Figure 46 illustrates how it is possible to obtain at the same time both the power fail and reset functions simply by adding one diode (D) and one resistor (R).

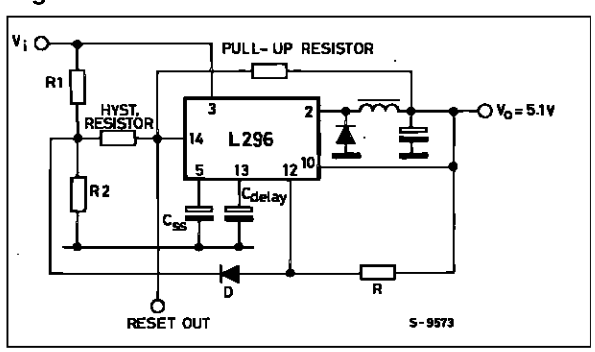
In this case the Reset delay time (pin 13) can only start when the output voltage is $V_O \geq V_{REF}$ - 100mV and the voltage accross R2 is higher than 4.5V.

With the hysteresis resistor it is possible to fix the input pin 12 hysteresis in order to increase immunity to the 100Hz ripple present on the supply voltage.

Moreover, the power fail and reset delay time are automatically locked to the soft-start. Soft-start and delayed reset are thus two sequential functions.

The hysteresis resistor should be In the range of aboit 100kΩ and the pull-up resistor of 1 to 2.2kΩ.

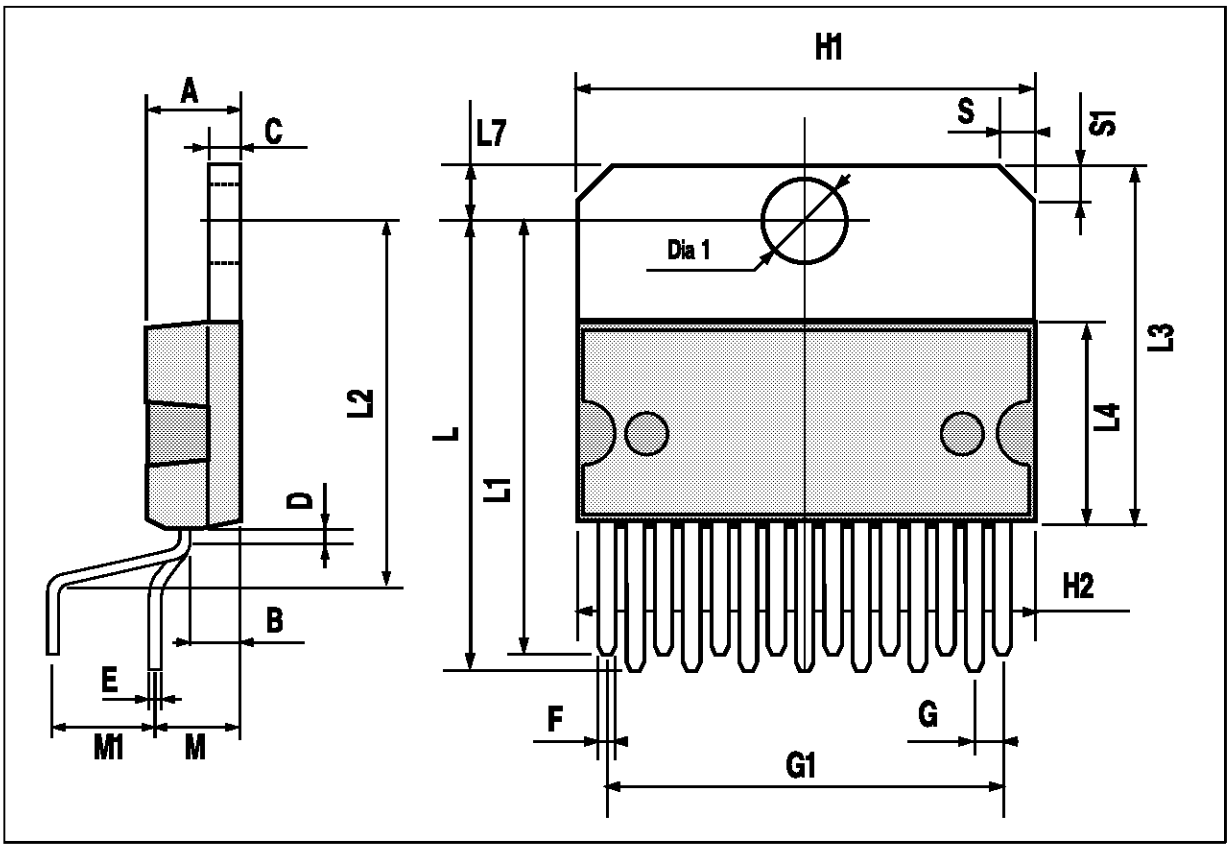
Figure 46



MULTIWATT15 VERTICAL PACKAGE MECHANICAL DATA

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5			0.197
B			2.65			0.104
C			1.6			0.063
D		1			0.039	
E	0.49		0.55	0.019		0.022
F	0.66		0.75	0.026		0.030
G	1.14	1.27	1.4	0.045	0.050	0.055
G1	17.57	17.78	17.91	0.692	0.700	0.705
H1	19.6			0.772		
H2			20.2			0.795
L	22.1		22.6	0.870		0.890
L1	22		22.5	0.866		0.886
L2	17.65		18.1	0.695		0.713
L3	17.25	17.5	17.75	0.679	0.689	0.699
L4	10.3	10.7	10.9	0.406	0.421	0.429
L7	2.65		2.9	0.104		0.114
M	4.2	4.3	4.6	0.165	0.169	0.181
M1	4.5	5.08	5.3	0.177	0.200	0.209
S	1.9		2.6	0.075		0.102
S1	1.9		2.6	0.075		0.102
Dia. 1	3.65		3.85	0.144		0.152

MUL15V.TBL



PMMUL15V.EPS